Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Cancelled)
Claim 2 (Cancelled)
Claim 3 (Cancelled)
Claim 4 (Cancelled)
Claim 5 (Cancelled)
Claim 6 (Cancelled)
Claim 7 (Cancelled)
Claim 8 (Cancelled)
Claim 9 (Cancelled)
Claim 10 (Cancelled)
Claim 11 (Cancelled)
Claim 12 (Cancelled)
Claim 13 (Cancelled)
Claim 14 (Cancelled)
Claim 15 (Cancelled)
Claim 16 (Cancelled)
Claim 17 (Cancelled)
Claim 18 (Cancelled)
Claim 19 (Cancelled)
Claim 20 (Cancelled)
Claim 21 (Cancelled)
Claim 22 (Cancelled)
Claim 23 (Cancelled)
Claim 24 (Cancelled)
Claim 25 (Cancelled)
Claim 26 (Cancelled)
Claim 27 (Cancelled)
Claim 28 (Cancelled)

Claim 29 (Currently Amended)

A content addressable memory device comprising:

rows of matchlines precharged to a voltage level corresponding to a miss condition, each of the rows of matchlines including a first matchline segment and a second matchline segment;

a first number of ternary cells connected in parallel to each of the first matchline segments ~~matchlines~~;

a second number of binary cells connected in parallel to each of the second matchline segments ~~matchlines~~, the binary cells being smaller in size than the ternary cells and operable simultaneously with the ternary cells; and,

matchline sense amplifiers connected to ~~each of~~ the first matchline segments and the second matchline segments ~~matchlines~~ for detecting one of the miss condition and a match condition of the first matchline segments and the second matchline segments in response to search data~~, each matchline sense amplifier providing a match output if data stored in the ternary cells and the binary cells of each row matches the search data~~.

Claim 30 (Previously presented)

The content addressable memory device of claim 29, wherein the ternary cells include SRAM based ternary content addressable memory cells.

Claim 31 (Previously presented)

The content addressable memory device of claim 30, wherein the binary cells include SRAM based binary content addressable memory cells.

Claim 32 (Previously presented)

The content addressable memory device of claim 29, wherein the ternary cells include DRAM based ternary content addressable memory cells.

Claim 33 (Cancelled)

Claim 34 (Currently Amended)
The content addressable memory device of claim 29, further including a third number of configurable ternary-binary content addressable memory cells connected in parallel to at least one of the first matchline segments and the second matchline segments~~each of the matchlines~~.

Claim 35 (Cancelled)
Claim 36 (Cancelled)
Claim 37 (Cancelled)

Claim 38 (Previously presented)
The content addressable memory device of claim 29, wherein the first number is selected to store at least a corresponding number of header bits.

Claim 39 (Cancelled)
Claim 40 (Cancelled)
Claim 41 (Cancelled)
Claim 42 (Cancelled)
Claim 43 (Cancelled)
Claim 44 (Cancelled)
Claim 45 (Cancelled)
Claim 46 (Cancelled)
Claim 47 (Cancelled)

Claim 48 (New)
The content addressable memory device of claim 29, wherein one matchline sense amplifier connected to the first matchline segment is configured to disable one matchline sense amplifier connected to the second matchline segment in response to the miss condition of the first matchline segment.

Claim 49 (New)

The content addressable memory device of claim 48, wherein the one matchline sense amplifier connected to the second matchline segment is configured to provide a match output if the first matchline segment and the second matchline segment have the match condition.

Claim 50 (New)

The content addressable memory device of claim 29, wherein the second matchline segment is at the voltage level corresponding to the miss condition when the first matchline segment is at the voltage level corresponding to the miss condition.

Claim 51 (New)

The content addressable memory device of claim 29, wherein the ternary cells connected to the first matchline segments are searched in a first search and compare cycle, and the binary cells connected to the second matchline segments are searched in a second search and compare cycle after the first search and compare cycle.

Claim 52 (New)

The content addressable memory device of claim 29, wherein one matchline sense amplifier connected to the second matchline segment is configured to disable one matchline sense amplifier connected to the first matchline segment in response to the miss condition of the second matchline segment.

Claim 53 (New)

The content addressable memory device of claim 52, wherein the one matchline sense amplifier connected to the first matchline segment is configured to provide a match output if the first matchline segment and the second matchline segment have the match condition.

Claim 54 (New)

The content addressable memory device of claim 29, wherein the first matchline segment is at the voltage level corresponding to the miss condition when the second matchline segment is at the voltage level corresponding to the miss condition.

Claim 55 (New)

The content addressable memory device of claim 29, wherein the binary cells connected to the second matchline segments are searched in a first search and compare cycle, and the

ternary cells connected to the first matchline segments are searched in a second search and compare cycle after the first search and compare cycle.

Claim 56 (New)

The content addressable memory device of claim 29, wherein the first matchline segment includes a third number of binary cells.

Claim 57 (New)

The content addressable memory device of claim 56, wherein the third number of binary cells are interleaved with the first number of ternary cells.

Claim 58 (New)

The content addressable memory device of claim 29, wherein the second matchline segment includes a third number of ternary cells.

Claim 59 (New)

The content addressable memory device of claim 58 wherein the third number of ternary cells are interleaved with the second number of binary cells.